PATENT
AUS9-2001-0301-US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Sang Hoo Dong et al.	)	
Serial No.: 09/915,437	)	Group Art Unit: 2825
Filed: July 26, 2001	)	
	)	Examiner: Binh C. Tat
FOR: METHOD OF LOGIC CIRCUIT SYNTHESIS AND DESIGN USING A DYNAMIC CIRCUIT LIBRARY	)	Confirmation No.: 7370

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

This paper is submitted in response to the Final Office Action mailed June 30, 2006, in the above-identified application, and is filed within the three-month shortened statutory period for response set in the Final Office Action.

Appellants request review of the final rejection in the above-identified application. No amendments are being filed with this request and this request is being filed with a Notice of Appeal. The review is requested for the reasons stated in the following remarks.

CLAIMS 1-18 ARE NOT ANTICIPATED BY THE YEE ARTICLE

Claims 1-18 stand rejected under 35 U.S.C. §102(b) as being anticipated by "Dynamic Logic Synthesis," IEEE, 1997, to Yee et al. ("Yee" or the "Yee article"). The Appellants submit that Yee does not anticipate claims 1-18 because Yee does not expressly or inherently disclose all of the limitations required by these claims.

The present application includes three independent claims, claims 1, 8, and 13. Due to the nature of the claims, claim 8 will be addressed first in the comments below.

Claim 8

Independent claim 8 is directed to a method for synthesizing a logic circuit providing a predetermined logical operation, and includes the following limitations:

(a) defining a logic synthesis block comprising a single dynamic logic circuit; and
(b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis utilizing a synthesis library constrained to the single dynamic logic circuit comprising the logic synthesis block.

A specific example of logic synthesis performed according to the requirements of claim 8 is found starting on page 7, line 6 of the present application. The discussion at page 10, line 15 to page 11, line 2 of the Appellants' response filed April 12, 2006 in this case describes how this specific example in the present application corresponds to the limitations of claim 8.

The issue which the Appellants request to be considered in this review with respect to claim 8 is whether Yee teaches performing logic synthesis utilizing a synthesis library constrained to a single dynamic logic circuit as required in element (b) of claim 8.

The Final Office Action references Figures 1-8 and pages 345-347 of Yee as disclosing element (b) of claim 8. However, there is no suggestion in the cited portions of Yee for

performing logic synthesis utilizing a synthesis library constrained to a single dynamic logic circuit. The only synthesis libraries specifically mentioned in Yee are mentioned at page 347, fourth full paragraph, which clearly describes synthesis libraries having several different types of logic circuits.

Because the Yee article does not teach or suggest the limitation set out at element (b) of claim 8, the Appellants submit that claim 8 is not anticipated by Yee and is entitled to allowance along with its respective dependent claims, claims 9-12.

Claim 1

Claim 1 requires limitations similar to those required by claim 8. However, rather than requiring that logic synthesis is performed utilizing a synthesis library constrained to a single dynamic logic circuit, element (b) of claim 1 requires that logic synthesis is performed with a synthesis library constrained to a particular logic synthesis block, that is, only one logic synthesis block. As discussed above in connection with claim 8, the Yee article discloses only synthesis libraries that include multiple blocks (specifically at least OR, NOR, and NOT gates as indicated at Yee, p. 347, col. 2, second full paragraph). Thus, the Yee article fails to disclose element (b) of claim 1.

Element (c) of claim 1 additionally requires producing a final circuit by eliminating unused devices in an intermediate circuit resulting after the logic synthesis constrained to the particular logic synthesis block. However, Yee does not disclose any unused devices after logic synthesis, nor does Yee disclose eliminating unused devices from an intermediate circuit as required by element (c) of claim 1. In contrast to the requirement in claim 1 relating to the removal of unused devices from an intermediate circuit, Yee discloses that after logic synthesis,

delay elements are added to the netlist to provide the correct self-timed delays and proper precharge-evaluation clock (See Yee at page 347, Fig. 7 and final paragraph).

Because Yee does not disclose at least elements (b) and (c) of claim 1, the Appellants submit that claim 1 is not anticipated by Yee and is entitled to allowance along with its respective dependent claims, claims 2-7.

Claim 13

Similarly to claim 1, independent claim 13 requires constraining a logic synthesis tool to a particular logic synthesis block, that is, a single logic synthesis block. As discussed above with respect to claim 1, the Yee article does not disclose this limitation. Because Yee does not disclose all of the limitations required by claim 13, the Appellants submit that Yee cannot anticipate claim 13 and that claim 13 is entitled to allowance along with its respective dependent claims, claims 14-18.

REJECTIONS OVER YEE HAVE BEEN APPLIED INCONSISTENTLY

The Appellants note that the rejections in view of the Yee article were originally made in the Office Action mailed March 29, 2005, but omitted in the Office Action mailed July 13, 2005, in favor of rejections over different art. Surprisingly, the claims were again rejected in view of Yee in the Office Action mailed January 13, 2006. The Appellants respectfully submit that the original rejections in view of Yee should have been withdrawn in the July 13, 2005 Office Action, and should not have been reinstated.

CONCLUSION

For all of the above reasons, the Appellants respectfully request reconsideration and allowance of claims 1-18.

Respectfully submitted,

The Culbertson Group, P.C.

Dated: 29Sept2006

By: _____

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